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High sensitivity magnetic built-in current sensor

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High sensitivity magnetic built-in current sensor

This invention relates to current sensors for sensing of current in a conductor, to integrated circuits having such a sensor built-in, to methods of using such sensors, and to methods for sensing current in a conductor in a semiconductor device such as an integrated circuit, amongst others as well as software products for implementing the methods of use.

There are various types of known BICS (Built In Current Sensor). Some are described in US 5,963,038, which shows detecting faults in integrated circuits by measurement of current through a conductor in the integrated circuit by means of a sensor situated in the vicinity of the conductor. The sensor can be constructed in various ways so as to measure the field produced by the current through the conductor. Examples disclosed include a Hall sensor, an MR (magnetoresistive) sensor and a GMR (giant magnetoresistive) sensor. This can enable testing of conductors and their connections which cannot be accessed easily by external test equipment, or for detecting faults in individual ones of parallel paths which would pass a resistivity test even if only one path was conducting.

An MR sensor has a resistance that is dependent on an external magnetic field in the plane of the sensor. Different types of MR sensors exist. Sensors based on anisotropic magnetoresistance (AMR), have been used in magnetic recording heads for several years. MR sensors have a layer of anisotropic magnetic material and the resistance of this layer is influenced by an external magnetic field, which causes the change in the sense current which flows in the layer. A GMR (Giant MagnetoResistive) sensor has a layer of magnetic material in a fixed direction (pinned layer) and a layer of magnetic material of which the magnetisation direction can be influenced by an external magnetic field (free layer), which causes the change in measured resistance. Depending on the type and construction, an MR sensor is more sensitive in one direction and less sensitive in another direction in the plane of the sensor. The MR sensor shown in the above patent is illustrated in Fig. 1. It is constructed to maximise the effect from the current through the conductor on the resistance of the sensor. Fig. 1 shows an MR (magnetoresistive) sensor 502 situated near conductor 104 in a layer of the integrated circuit above or beneath the layer in which the conductor is realised. The MR

sensor 502 comprises connection areas 504 and 506 to which through holes 508 and 510 are connected for measuring the actual resistance of the sensor 502.

The current through the conductor 104 causes a circular magnetic field around the conductor 104 through the plane of the sensor 502 and perpendicular to the conductor 104 in the plane of the sensor 502. The MR sensor 502 is sensitive in this direction, so its resistance is measured along the plane of the sensor 502, parallel to the conductor plane to measure the strength of the magnetic field produced by direct current through the conductor 104. A traditional MR sensor or a GMR (giant magnetoresistive) sensor can be used.

Fig. 2 shows an alternative arrangement of the MR sensor in the integrated circuit known from the above patent. An MR sensor 602 is situated near the bond pad 106 to which the bond wire 108 is connected. The MR sensor 602 has connection areas 604 and 606 for connecting the sensor 602 to respective through holes 608 and 610. The typical attachment of the bond wire 108 to the bond pad 106 is such that near the bond pad 106 the bond wire 108 is to a certain degree perpendicular to the surface of the bond pad 106. A current through the bond wire 108 then causes a magnetic field 612 in the plane of the bond pad 106 and the MR sensor 602, thus causing a change of the resistance of the MR sensor 602. A second MR sensor 614 may be situated at another side of the bond pad and combined with the MR sensor 602 in order to obtain an arrangement that is more sensitive to the magnetic field 612 than a single MR sensor. In Fig. 2, the MR sensors are positioned perpendicular to the magnetic field 612. They may be positioned at different angles to the magnetic field according to which position is more sensitive. In any case, the resistance of the sensor layer is still measured along the plane of the layer.

At a connection layer of the circuit, the through holes e.g. 508-510 and 608-610, are connected to connection tracks connecting the respective MR sensor 502, 602 to an internal detection circuit or to external measurement points. The resistance of the MR sensor 502, 602 can then be measured inside in the integrated circuit with the detection circuit or outside the integrated circuit with a suitable measurement arrangement.

Such sensors are useful for sensing high currents, but are not sufficiently sensitive for applications such as Quiescent Current (IDDQ) testing. IDDQ testing has shown very good coverage of physical defects such as gate oxide shorts, floating gates, and bridging faults which are not very well modelled by classical fault models, or undetectable by conventional logic tests. The demand for high quality and cost effectiveness has led to widespread use of IDDQ testing as a supplementary test to voltage tests. When combined with other test techniques, it has the potential for eliminating the need for burn-in test.

However MOSFET leakage currents are rising rapidly with each technology node, narrowing the difference between the IDDQ levels of a faulty and fault-free circuit.

It is an object of the present invention to provide a sensor which is sensitive enough to measure small current on-chip such as IDDQ currents for testing.

In a first aspect, the present invention provides a semiconductor device with a conductive element and a current sensor. The current sensor is a magnetic current sensing device for sensing direct, varying or alternating current flowing through the conductive element. The current sensing device is integrated in the semiconductor device and is galvanically isolated from the conductive element. An advantage is greater sensitivity of the sensor compared to prior art sensors: the sensor may be suitable for measuring current with a μA resolution. The greater sensitivity enables less signal post processing and electronic circuitry to be used, which is important for applications such as mobile devices. Notably sufficient sensitivity can be obtained in principle for IDD measurements such as quiescent IDD current (IDDQ) or transient IDD current (IDDT), even for next generation CMOS processes which have more stringent IDD test requirements. IDDQ is the quiescent current flowing from Vdd to Vss (IDD current) in CMOS circuitry, in a quiescent state. IDDT is the transient IDD current during digital transitions. Measuring the IDDQ and IDDT currents allow to detect faults within the CMOS circuitry.

The current sensing device may comprise at least one magnetoresistance device, such as a magnetic tunnel junction (MTJ) device, exhibiting the tunnel magnetoresistance (TMR) effect. In this embodiment, the sensor can provide easy integration with next generation CMOS processes such as MRAM technology. It can be more compact, and uses less power than prior art sensors.

The magnetic tunnel junction (MTJ), which according to an embodiment of the present invention may be used as a sensing element, has been developed previously for memory applications, and the inventors have appreciated that it could be adapted for use as a sensor, despite the fact that memory cells and current sensors must have different characteristics. In a memory cell, a magnetoresistance loop (MR loop) of a free layer should be square with a relatively large coercivity (in the order of a few tens of Oe) and having two distinct remanence states. Moreover, the centre of the loop must be at zero field. In contrast, a current sensor must have on the one hand as large susceptibility to magnetic field as possible

(for high sensitivity) and on the other hand must have small or no hysteresis and linear characteristic within the measuring range.

The current sensing device may be arranged to have a relationship between resistance and magnetic field which shows substantially no hysteresis.

The current sensing device may have a free magnetic layer which has an easy axis oriented at an angle between 70° and 110°, preferably to be substantially perpendicular to a field being measured, so as to minimise the hysteresis. The current sensing device may have an easy axis, wherein the easy axis of the free layer is caused by shape elongation.

The current sensing device may have a pinned magnetic layer with a magnetisation direction and a free magnetic layer having an easy axis, wherein the magnetisation direction of the pinned magnetic layer is oriented at an angle, with the easy axis of the free magnetic layer, preferably between 0° and 180°, more preferred between 45° and 135°, and still more preferred substantially perpendicular to the easy axis of the free magnetic layer, so to maximize the sensitivity of the signal to be measured. In order to suppress the hysteresis, the present invention includes deviations from this angle of 90°.

The current sensing device may be subjected to an additional, direct or constant magnetic field created by e.g. a second current in the vicinity of the device either to further suppress the hysteresis, when the additional field is applied substantially perpendicular to the field being measured, or to shift the measurement range, when the additional field is applied substantially parallel to the field being measured.

Alternatively, the current sensing device may be subjected to an additional alternating field created by the second current. The additional alternating field is used to modulate the field to be measured thus modulating the sensor signal. The signal to noise ratio can be then improved by using signal processing methods.

The semiconductor device according to the present invention may comprise a sensor device which is compatible with CMOS or MOS processing.

The semiconductor device may be an integrated circuit.

The present invention also includes software products, which when executed on a procesing device, implement applications using measured currents in accordance with the present invention.

Additional features which form dependent claims include the sensor element being planar and the tunnel current being detected perpendicular to the plane of the planar element. Another such feature is the element being arranged to have a relationship between resistance and field, which shows substantially no hysteresis. Another such feature is that the

sensor element has a free magnetic layer which has an easy axis oriented at an angle, preferably between 70° and 110°, more preferred substantially perpendicular to the field being measured. This angle should preferably be close to 90° in order to be able to have the highest (absolute) signal and lowest hysteresis. Otherwise only the component along the 90° direction is measured. This explains why extra modulation or biasing schemes would be allowed in the perpendicular direction. Another such feature is that the junction comprises a pinned magnetic layer having a magnetisation oriented at an angle, preferably between 45° and 135°, more preferred substantially perpendicular to the easy axis of the free magnetic layer. Another such feature is that the detection circuitry comprises circuitry for applying a fixed voltage across the junction of the sensor element, and for feeding the tunnel current through a load, and an amplifier for amplifying the voltage across the load. Another such feature is that the detection circuitry comprises circuitry for actively clamping the voltage across the junction. Alternatively, the detection circuitry can work in a current mode in which a constant current supplied by a current source flows through the junction and the change in the voltage drop on the junction is the indication of its resistance change and an amplifier is used to amplify this voltage. Clearly the output can be anything from a logical signal indicating field detected or not, to an analog or digital signal indicating a measurement to a given level of precision. Suitable post processing of the detected output can be carried out to suit the precision or noise immunity of the application for example.

As an additional feature, a width of the sensor element in a direction parallel to a width of the conductor, should be not larger, preferably less, than the width of the conductor. This can help to ensure a uniform field through the sensor.

Another aspect of the invention provides a sensor for sensing a magnetic field, having a magneto resistive sensing element with crossed anisotropy, i.e. the angle between the free magnetic layer and the pinned direction of the pinned magnetic layer is substantially 90°, such that an axis of elongation of the sensing element is substantially orthogonal to the magnetic field being sensed, i.e. includes an angle between 70° and 110°, preferably substantially 90° between the free magnetic layer and the field being sensed.

Another aspect provides an integrated circuit having a built in current sensor comprising a magnetoresistive current sensor with a sensitivity of greater than 100μV per mA.

Another aspect provides an integrated circuit having a built in current sensor comprising a magnetoresistive current sensor arranged to sense quiescent current (IDDQ).

Another aspect provides corresponding methods of sensing magnetic field or of sensing current.

In a second aspect, the present invention provides the use of an integrated magnetic current sensing device which is galvanically not in contact with a conductive element, for sensing at least a direct, a varying or an alternating current flowing through the conductive element, wherein the sensing device is used for on-chip measurement of current.

The current sensor or sensors may be arranged to sense quiescent currents (IDDQ) or transient currents (IDDT). As an additional feature, the integrated circuit may have multiple current sensors of which the outputs are linked in a scan chain based mechanism such as boundary scan (IEEE standard 1149.1). An advantage of a current sensor in a semiconductor device according to the present invention is that it has a small physical size. Being small, it can easily be integrated in an IC. This built-in sensor makes the IDDQ measurement possible per circuit block inside an IC or per separately powered circuit in a constellation of circuits in a single package, like an MCM (multichip module) or MCP (multichip package). Also IDDT measurement per block becomes possible. With the expectation of further growing integration levels in the IC domain, this will be an important test and measurement capability.

Furthermore, when integrated, more functionality can be added for these sensors.

As an additional feature, the integrated circuit may have multiple current sensors of which the outputs are linked in a scan chain. The invention makes it possible to use a multitude of sensors to measure currents as consumed by different blocks to determine the part of the design that consumes too much or too little current. Faster debugging of the initial design is a key economic benefit. Additionally, wear-out of the IC during its life time can now be monitored. Looking for changes in current consumption during the actual life time may prevent unexpected failures. Among others, safety aspects for life-critical applications can be derived from this data.

Another capability is the measurement of the current in separate processing units or cores. The method may comprise measuring current in at least one processing module. The function is to determine the scheduling of tasks based on dynamic power distribution schemes. The cores are processing units that consume power and may get hot when running at their maximum capacity. Based on the current (power) measurement per processing unit, a more even processing load can be scheduled, especially in systems that have many parallel processing units. This prevents unnecessary waiting queues, but also

excessive heat build up in a specific core may be prevented. Also power reduction schemes may be controlled in this way, thus preventing expensive heat transfer solutions at assembly level.

A novel, now feasible technique, is the control of the clock speed of at least one processing module to obtain a continuous matching with a pre-defined current consumption level. This will give a maximum performance versus battery life capability.

For this technique to work properly, the threshold levels for comparing the power consumption must be set in registers by software. This software can be a service routine that is closely matched with an operating system. The job scheduler part of the software must be capable of rescheduling, based on interrupts from the detection or from regular reading (polling) the values from registers. This hardware controlled aspect is relatively new in scheduling software but is basically not different from software based scheduling that already exists.

In a third aspect, the present invention provides a method for sensing current in a conductor in a semiconductor device. The method comprises sensing a direct, a varying or an alternating current flowing in the conductor by performing contactless magnetic current sensing with a sensor integrated on the integrated circuit.

The method may comprise sensing a magnetic field caused by the current.

The present invention also provides a method comprising the measurement of current consumption and the generation of a warning signal if a pre-set current consumption threshold is superseded.

The present invention furthermore provides a method wherein a software based routine performs job scheduling over several processing units based on the measured currents that invoke either an interrupt or a register bit to be set.

The features of any of the dependent claims can be combined with each other or with any of the independent claims. Further advantages will be apparent to those skilled in the art, especially over other prior art not known to the inventors. How the present invention may be put into effect will now be described with reference to the appended schematic drawings. Obviously, numerous variations and modifications can be made without departing from the claims of the present invention. Therefore, it should be clearly understood that the form of the present invention is illustrative only and is not intended to limit the scope of the present invention.

The features of the invention will be better understood by reference to the accompanying drawings, which illustrate preferred embodiments of the invention. In the drawings:

Figs. 1 and 2 show prior art sensors,

Fig. 3 shows a prior art MTJ memory cell,

Fig. 4A illustrates a CMOS inverter, and Fig. 4B illustrates IDDQ current for non-defect and for defect circuitry when the input voltage Vin of the CMOS inverter of Fig. 4A changes from low to high,

Fig. 5 shows a graph plotting the IDDQ current measured after a number of test patterns are applied to the digital inputs of the circuitry,

Fig. 6 shows a schematic view of a sensor according to an embodiment of the present invention,

Figs. 7A, 7B and Figs. 8A, 8B show magneto resistance characteristics for a given prior art memory cell structure and a sensor structure according to an embodiment of the present invention, respectively,

Fig. 9 shows a voltage versus current to be measured characteristic of a TMR sensor,

Fig. 10 shows a graph of magnetic field strength varying with distance from the conductor for various conductor widths,

Figs. 11 and 12 show orientations of layers of a prior art memory cell and a sensor according to an embodiment of the present invention, respectively,

Figs. 13 to 16 show graphs of resistance of a TMR element against magnetic field strength in different situations,

Figs. 17 and 18 show readout circuits for sensors according to embodiments of the invention,

Fig. 19 illustrates a basic current detection scheme according to an embodiment of the present invention,

Fig. 20 illustrates a system on chip (SOC) where the applied core blocks all have a current sensor that may be a set of distributed sensors per core, and

Fig. 21 illustrates a system on chip (SOC) where the output from the current sensors in the applied core blocks is connected to a task scheduler.

The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. Where the term "comprising" is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun e.g. "a" or "an", "the", this includes a plural of that noun unless something else is specifically stated.

By way of introduction to the description of embodiments of the invention, MRAM development will be explained briefly. During recent years, research into Magnetic RAM (MRAM) has been intense. The integration of magnetic materials with CMOS technology has become less of a problem. Commercial MRAM production is planned in 2004-2005. A survey of MRAM technology is presented by K.-M.H. Lenssen et al, "Expectations of MRAM in comparison.", Non-Volatile Memory Technology Symposium 2000, (Nov. 15-16,2000, Arlington VA, U.S.A.). This shows that first generation Magnetic Random Access Memory (MRAM) were based on AMR. After 1988 the discovery of a larger magnetoresistance effect called giant magnetoresistance (GMR), enabled the realisation of smaller elements with a higher resistance and a larger MR effect (5 to 15%), and therefore a higher output signal. This enabled, in principle, MRAMs for general applications. A decade after its discovery the GMR effect is already applied in commercial products like HDD read heads and magnetic sensors.

A breakthrough in the field of magnetic tunnel junctions around 1995 improved the prospects of MRAM even further, when a large tunnel magnetoresistance (TMR) effect was demonstrated at room temperature. Since then TMR effects with amplitudes up to >50% have been shown, but because of the strong bias-voltage dependence, the useable resistance change in practical applications is at present around 35%.

An example of a cell for such a device is given in Fig. 3. This structure and how to manufacture it is well known and need not be described again in detail here. To summarise, such a TMR-based MRAM contains cells which are magnetic tunnel junctions (MTJs). MTJs basically contain a free magnetic layer 102, an insulating layer (tunnel barrier) 103, a pinned magnetic layer 105 and an antiferromagnetic layer 107 which is used to "pin" the magnetisation of the pinned layer 105 to a fixed direction. In the example shown in Fig. 3, there is a layer structure having, in order, a top contact 100, a free magnetic layer 102,

a tunneling barrier 103, a fixed magnetic layer 105, a pinning layer 107, and a bottom contact 110.

The MRAM cells store binary information (1/0) in the directions of magnetisation of the free magnetic layer 102, which can be relatively free to rotate between two opposite directions. The resistance of the MTJ is small if the direction of magnetisation of the free layer 102 is parallel with that of the pinned layer 105 and is large when they are antiparallel. For reading information on a certain cell, a small sense current Is is sent through the MTJ stack (vertically) of the selected cell. The measured voltage drop on the MTJ (proportional to the resistance) is the indication of the information of the cell. The information on a cell can be changed during a write operation by sending write currents through word lines and bit lines, which are patterned at the bottom and on top of the memory cells. The currents will create magnetic fields (easy axis field and hard axis field) in the memory cell. The fields are programmed so that they are large enough to switch the magnetisation of the free layer 102 of the selected cell to a new direction, depending on the binary information to be stored into the selected cell.

In general, both GMR and TMR result in a low resistance if the magnetisation directions of the free layer and the pinned layer are parallel, and in a high resistance when the orientations of the magnetisation are antiparallel. In TMR devices the sense current has to be applied perpendicular to the layer planes (CPP, Current Perpendicular to Plane) because the electrons have to tunnel through the barrier layer. In GMR devices the sense current usually flows in the plane of the layers (CIP, Current In Plane). Nevertheless, supported by the rapidly continuing miniaturisation, the possibility of basing MRAMs on CPP TMR seems more likely.

The inventors have appreciated that MTJ devices can be adapted for use as magnetic field sensors. These have many applications, for example in contact-less measurements of currents flowing through a conductive element, e.g. power current or IDD current, contact-less being with respect to the conductive element. This can be in any kind of CMOS chip or other chip. Of course it can be implemented in MRAM chips. The same manufacturing technology used for MRAM cells can be used with little change, to build integrated current sensors according to embodiments of the present invention. They are particularly suitable for power pin testing and IDDx testing in MRAM chips or chips containing embedded MRAM, since implementation of these sensors may not need to cost any extra mask or extra process steps.

In CMOS circuitry, for instance the CMOS inverter as shown in Fig. 4A, IDD is the current flowing from a high power supply level Vdd to a low power supply level Vss. When the circuitry is idle, meaning that there are no digital transitions within the circuitry, also called the quiescent state, IDD current is stable and has a small value called the quiescent IDD current or briefly IDDQ current. When there are any digital transitions taking place in the circuitry, such as e.g. V_{in} changing from low to high and consequently V_{out} changing from high to low (Fig. 4B, upper part), IDD current raises to a maximum called the transient IDD current or briefly IDDT current (Fig. 4B, middle and bottom part). Then, after the transition, it falls back again to the quiescent IDDQ level (Fig. 4B, middle part). The mentioned situation occurs when the circuitry is free of defects. In case there are any defects such as gate oxide shorts, floating gates, bridging faults, etc., as indicated by, for example, the parallel resistor R_p in Fig. 4A, a significant increase in the IDDQ after transition is observed, as illustrated in the bottom graph of Fig. 4B. By monitoring the IDDQ current after transitions, defects of the circuitry can easily be detected.

IDDQ has been proved to be a very good testing method, which can cover a lot of faults not detected by other methods so far.

An improved method of IDDQ testing is the delta IDDQ method. In the delta IDDQ testing method, a number of test patterns are sent to the digital inputs of the circuitry and the IDDQ is monitored and compared (Fig. 5). The patterns are designed so that it guarantees to change the value (toggle) of every internal net. The difference between the mean value of one pattern to another is called ΔIDDQ. If any of the ΔIDDQ values departs too much from the known normal value, it can be concluded that the circuitry is defective.

For both methods, the current resolution preferably is a few μA or less; even though the current range in the delta IDDQ method can be in the mA range or even more, depending on the size of the circuitry. More information on IDDQ testing can be found in Bram Kruseman et al, The future of delta IDDQ testing, Proceedings of the Test Conference, 2001, Pages 101-110, which is incorporated herewith by reference.

The basic principle of a sensor according to an embodiment of the present invention is shown in Fig 6. Fig. 6 shows that the sensor has three layers, a free magnetic layer 102, a tunneling barrier 103, and a pinned or fixed magnetic layer 105. The current I_x to be measured is sent through a conductor line 200, which is located underneath the MTJ sensor element 210. The sensor element 210 is galvanically isolated from the conductor 200 using a conventional isolating layer (not shown in Fig. 6). The sensor element 210 is elongated along the axis of the conductor 200, as discussed in more detail below. The sensor

element 210 can be patterned in exactly the same way as MRAM cells and may be located outside the area containing the memory array. The field created by the current I_x will rotate the magnetisation direction of the free layer 102 of the sensor element 210, which can be detected by its resistance change. A sense current I_s is sent through the element 210 (from top to bottom) to measure the resistance.

In spite of using a similar principle, MRAM cells and current sensors according to embodiments of the present invention have different characteristics, as shown in Figs. 7A and 8A. In each case, the corresponding orientation of magnetic layers is shown in Figs. 7B and 8B. Fig. 7A shows resistance versus magnetic field characteristics for an MRAM memory cell structure. In MRAM cells, it is desired that the magnetoresistance loop (MR loop) of the free layer be square with a relatively large coercivity (in the order of a few tens of Oe) and having two distinct remanence states. Moreover, the centre of the loop must be at zero field. In contrast, as shown in Fig. 8A, the characteristic for the current sensor is quite different. It must have on the one hand a sloping characteristic to give as large a susceptibility to magnetic field as possible (for high sensitivity) and on the other hand must have small or no hysteresis. The centre of the loop does not need to be at the zero field. Depending on applications the centre point can be chosen. For instance it can be shifted in the direction of the measured field so that its detected range is broadened in case of measuring wide-range unidirectional current.

The geometry-dependence of the magnetic behaviours of the elements can be exploited to build the sensors with the desired characteristic. In MRAM, to obtain the mentioned hysteresis loop, the easy axis of the free layer must be parallel with the direction of the pinned magnetisation as shown in Fig. 7B. In these Figs. 7B and 8B, the free layer and the pinned layer are shown slightly offset for the sake of clarity. In practice, the layers should be stacked on top of each other, separated by a thin isolating layer (tunneling barrier). The easy axis can be achieved by patterning the element into an elongated shape, thus causing a shape anisotropy in the elongated direction. During writing, the easy axis field, which is the essential applied field component to switch the element, is directed along the easy axis.

In sensor configuration, the easy axis of the free layer (normally in the elongated direction) should be at an angle between 0° and 180°, preferably between 45° and 135° and more preferably substantially perpendicular to the pinned magnetisation, as shown in Fig. 8B. The conductor 200 for measured current I_x is preferably parallel with this easy axis, which will create a field perpendicular to the easy axis. It is well-known from the Stoner-Wohlfarth theory that the hysteresis loop of a single-domain magnetic element would

have no hysteresis if it is subjected to a magnetic field directed perpendicular to its easy axis. However it is not excluded that the measured current Ix is oriented at an angle with the easy axis; even though, in most cases the parallel arrangement is the optimum choice.

Furthermore, to suppress hysteresis further, the sensor may be subjected to an additional dc magnetic field (a few Oe) created by e.g. a second current conductor in the vicinity of the device to further suppress the hysteresis. The second current is arranged so that the direction of the additional field is substantially perpendicular to the field to be measured, thus substantially parallel to the easy axis of the free layer. The additional field stabilizes the coherent rotation of the magnetisation inside the free layer, thus suppressing hysteresis caused by domain wall motions. To shift the measurement range of the sensor, the second current can be arranged so that the direction of the additional field is substantially parallel to the field to be measured.

Alternatively, the sensor may be subjected an additional alternating field created by a second current conductor. The additional alternating field is used to modulate the field to be measured thus modulating the sensor signal. By using a suitable post signal processing method, the signal can be extracted, whereby signal to noise ratio can be significantly improved.

Fig. 9 shows a measurement of transfer characteristic (voltage versus current) of a TMR sensor element 210 having a size of 5 x 0.7 μm^2 (aspect ratio of 7). The distance between the sensor plane to the top of the conductor 200 is 100 nm. The conductor cross-section is 0.7 μm (lateral) x 0.32 μm (vertical). The sense current that flows through the MTJ is 11 μA and the voltage drop on the junction is about 200 mV, which is the value normally used to bias the MRAM cells. The resistance of the sensor is therefore about 18 kΩ. The linear part extends over a range of about 10 mA. The full magnetoresistance change (MR ratio) is about 23%. It should be noted here that the maximum MR ratio of this sensor measured at low bias voltage is in fact larger (about 30%); however in this case some MR ratio is sacrificed for a higher readout voltage. From the slope of the MR curve, the sensitivity of this sensor can be derived, which is 2.43 mV/mA or 1.3%/mA. For IDDx testing, the required resolution of 2 μA would result in a change of 4.86 μV. With an amplifier following conventional principles this change can easily be resolved without being swamped by noise.

The size of the sensor element 210 is more or less defined by the width of the conductor 200 which conveys the current to be measured. To have a relatively homogeneous field over the element 210, it is advisable that the width of the sensor element 210 be equal to

or smaller than the width of the conductor 200. On the other hand, the width of the conductor 200 must be chosen so that it provides enough field on the sensor element 210. Fig. 10 shows the relation between the conductor width and the conductor-sensor distance with the field created at the sensor element 210. The conductor 200 has a thickness of 300 nm and the current is 10 mA. Generally speaking, the smaller the width of the conductor 200 and the shorter the conductor 200 - sensor element 210 distance, the larger is the field that can be created. For instance, if a measurement of a few mA range is required, the width of the conductor 200 should not be larger than about 2 μm to get enough field to drive the sensor element 210. The thickness of the conductor 200 is taken to be about 300 nm and the distance between the conductor 200 and the sensor plane is about 150 nm, which are realistic practical values. Therefore since the width of the sensor element 210 should not be larger than that of the conductor 200, the sensor width should also be less than 2 μm.

The length of the sensor element 210 depends on the requirement of sensitivity and hysteresis. The smaller the aspect ratio, the larger is the sensitivity that can be obtained. Ideally the sensor shape can be round to get the maximum sensitivity. However, sensitivity is a counter factor of hysteresis: the smaller the aspect ratio, the larger the hysteresis becomes. To reduce hysteresis, it is necessary to induce some anisotropy along the conductor direction to stabilise the magnetic moments. The easiest way is to elongate the element to make use of the so-called "shape anisotropy". In practice, a compromised value of the aspect ratio is found to be about 5-7 (valid for elements having a width of about 1 to a few microns) to have a relatively high sensitivity without remarkable hysteresis.

Fig. 11 shows the orientation of the pinned (hard reference) layers and free (soft storage) layers in the memory cell, and Fig 12 shows the orientation of the corresponding layers for the sensor. Figs. 11 and 12 show how the shape anisotropy, in other words elongation, is orthogonal to the externally applied field H_{extern} for the sensor, yet is parallel for the prior art memory cell. This also produces the slope of the field transfer curve. In Fig. 12, a crossed-anisotropy configuration is achieved in the sensor design, which allows a stable magnetisation configuration (approximately at zero magnetic field) in which the magnetisation of soft and reference layers are orthogonal to one another.

Some examples of calculated characteristics are shown in the graphs of Figs. 13 to 16. Graphs illustrating resistance versus magnetic field strength are shown. Fig. 13 shows resistance versus magnetic field strength for a memory cell for reference purposes. It can be seen that sensitivity near zero field is low, and that there is hysteresis. This example used layers in a rectangular shape of 180 x 120 nm^2. The MRAM has a reference stack of

CoFe-Ru-CoFe of 1.75-2.25 nm, and a soft layer of NiFe of 5 nm. The CoFe-Ru-CoFe stack is called Artificial Antiferromagnetic (AAF) structure, in which the two magnetic layers (CoFe) are antiferromagnetically coupled through the non-magnetic layer Ru. This stack is in fact equivalent to a single pinned layer but more robust due to the strong antiferromagnetic interaction of the layers. Furthermore, it is to be noted that more advanced layered structures can be used for the free layer, in accordance to the material systems that have been introduced to improve the scalability of MRAM towards smaller CMOS nodes, such as magnetostatically coupled structures, and antiferromagnetically coupled AAF structures.

Fig. 14 illustrates the graph of resistance versus magnetic field strength for a first sensor device which is composed as the memory cell described above with respect to Fig. 13, and has dimensions 120 x 180 nm^2. In the sensor configuration, the magnetic layers CoFe of the reference stack are pinned to the direction which is orthogonal to the easy axis of the free layer and the field is applied in the direction of the pinning direction.

For an ellipse, the shape anisotropy is given by an anisotropy field

$$H_K = 4\pi\,(t.M)\,(\eta_y-\eta_x) / w,$$

with (t.M) the product of free layer thickness and saturation magnetisation, and $(\eta_y-\eta_x)$ a monotonously increasing function of the aspect ratio l/w with value 0 for $l / w = 1$ (circular) and 1 for $l / w = \infty$. For the numbers as given below, $H_K = 160$ Oe. The sensor sensitivity is then related to the signal. As an example, take a magnetic tunnel junction with e.g. 40 % usable TMR signal. The estimated sensitivity is then:

$$\text{Sensitivity} = \text{TMR}[\%] / (2.H_K)$$

For the example as given, there is a sensitivity of 0.125 %/Oe. Note that this sensitivity can be improved by increasing the width w of the sensor. An effective magnetic field sensitivity can be deduced from the voltage signal that is retrieved. For a bias of approximately 200 mV, a 40 % TMR signal leads to $\Delta V = 80$ mV, from which the sensitivity is calculated to be 250 μV / Oe before amplification. As in MRAM memory cell designs, a voltage-clamping transistor can be added, to fix the voltage V_{bias} over the sensor element, and the resulting current variation i_{sense} can be amplified. For a magnetic tunnel junction of 10 kOhm, the maximum current variation would be 8.3 μA, and with e.g. $R_{load} = 50$ kOhm, then $\Delta V = 415$ m V.

Fig. 15 illustrates the graph of resistance versus magnetic field for a second sensor device. The device has dimensions of 700 x 5000 nm^2, which are the same as the experimental sensor shown in Fig. 9. The device has a reference stack of CoFe-Ru-CoFe of

2.0-2.5 nm, and a soft layer of NiFe of 5 nm. Assuming that the full MR ratio is 40 %, it can be calculated that the sensitivity of the sensor is 0.4 % / Oe.

In a last step, the magnetic field generation of a current line can be considered. This problem heavily depends on the geometry as shown in Fig. 10. A typical value in MRAM designs is a few Oe magnetic field generation per mA current. Suppose a field generation of 5 Oe per mA. With the previous findings, this would lead to an effective current sensitivity of approximately 6.5 m V/mA. For the example as given in Fig. 16, using a rectangular sensor of 240 x 360 nm^2, where $H_K = 50$ Oe, there would be a current sensitivity of about 21 mV/mA, using the same assumptions.

In conclusion, from both experiment and theoretical considerations, it is possible to yield signals in the range of a few to a few tens of mV per mA, which would be about two orders of magnitude better than for current MAGFET devices as described in Walker et al, "A Practical Built-in Current Sensor for IDDQ Testing", ITC2001, paper 14.3; or in Giovanni Busatto et al, Microelectronics Reliability 43 (2003) 577-583. In other words, current variation in the μA level would lead to a change in signal in the μV to tens of μV range.

Any suitable conventional circuitry can be used as the detection circuitry for measuring the resistance of the sensing element, to suit the application. For high performance applications, two alternative readout circuits are presented in Figs. 17 and 18, which are in principle the same as readout circuits for MRAMs. As shown in Fig. 17, an op-amp 320 is used to amplify a voltage seen across a load resistor 310, which is coupled in series with the sensor 330, via a bias transistor 340. In Fig. 17, the bias voltage on the sensor is clamped to a relatively fixed value (about 200mV) and the change in resistance of the sensor causes a change in current, which results in a voltage change on the load resistor. This voltage change is then amplified. A disadvantage of the circuit is that it results in some variation of the clamping voltage when the resistance of the sensor is changed.

In Fig. 18, an improved circuit is presented, using material from US-6,205,073 Bl, in the context of MTJ memory readout. In this design, there are two op amps. An output op-amp 360 amplifies the output of a bias control op-amp 350. The bias control op-amp output is also fed to an input of the bias transistor 340. A negative input of op-amp 350 is fed by the voltage across the sensor. In this design, the negative feedback of the bias control op-amp allows an active way of clamping the voltage on the sensor 330, which can offer a more stable signal and faster readout time.

The output V_{signal} of the sensor module 390, which for example resembles the circuit shown in Fig. 17 or 18, can be read out, as illustrated in Fig. 19, through a sensor read-out amplifier 400, that has a second input V_{thres} to make a comparison possible with a pre-determined threshold. (in Fig. 19, the comparison signal originates from control logic 402 and may even be a programmable level). The resulting higher or lower signal is basically a digital signal and can preferably be transferred to an output pin by means of e.g. a boundary scan set up using internal registers according to the IEEE standard 1149.1 (Fig. 19).

The invention makes it possible to use a multitude of sensors to measure currents as consumed by different blocks to determine the part of the design that consumes too much or too little current. Fig. 20 illustrates a system on chip (SOC) 500 where the applied core blocks 502 all have a current sensor units 504 (that may be a set of distributed sensors per core). The sensor units 504 are connected to an access means (preferably a boundary scan set up like in Fig. 19). The check capability may be an additional processing function on this chip (not represented in the drawing). Through boundary scan, the check capability may also be placed outside the chip. Wear-out of the IC during its life time can be monitored. A more specific example is given in Fig. 21, in which current sensors are positioned on the power supply lines of at least one processing module or core. The power distribution network has been shown in a simplified form and would normally be much more complex than that schematically shown in Fig. 20 and 21. The outputs of the current sensors 504 are fed into a central task scheduler 700. The function of the scheduler 700 is to gather information about the power consumption of different modules or cores 502 then determine the scheduling of tasks based on dynamic power distribution schemes. The scheduler may be implemented in software running on a suitable processing device such as a conventional microprocessor, e.g. an embedded microprocessor or programmable digital logic device such as a Programmable Gate Array, e.g. Programmable Array Logic, Programmable Logic Array, Field Programmable Gate Array or similar. The cores 502 are processing units that consume power and may get hot when running at their maximum capacity. Based on the current (power) measurement per processing unit, a more even processing load can be scheduled, i.e. the task scheduler 700 can perform load balancing. Loading controls are then fed back to the cores 502. This functionality is especially useful in systems that have many parallel processing units. This prevents unnecessary waiting queues, but also excessive heat build up in a specific core 502 may be prevented. Also power reduction schemes may be controlled in this way, thus preventing expensive heat transfer solutions at assembly level. In other examples (not shown), the task scheduler 700 can be replaced by different circuitries which

have different functionalities such as a measurement unit or an interrupt generator. From there, a contact will be made either to an internal block or to the outside world or to a software environment for further work such as other control or monitoring jobs.

The current sensors described in any of the embodiments above can be implemented in integrated circuits of many kinds, particularly CMOS circuits and MRAM circuits. Outputs of such sensors can be coupled in scan chains following established practice, to multiplex many sensor outputs onto one or more outputs of the integrated circuit. Such integrated circuits can be used in conventional consumer equipment, particularly mobile devices such as laptop computers, mobile phones and safety systems such as ABS for cars and avionics and so on. As has been described above, a sensor for detecting magnetic field strength created by the current to be measured, has a sensor element using a magnetic tunnel junction, and detection circuitry, the sensor element having a resistance which varies with the magnetic field, the sensor element comprises a tunnel junction, and the detection circuitry is arranged to detect a tunnel current flowing across the tunnel junction. Anisotropy, such as caused by elongation, is oriented at an angle, preferably orthogonal to the magnetic field. Advantages include greater sensitivity, and thus less susceptibility to noise. Also it can provide easy integration with next generation CMOS processes, be more compact, and use less power. The greater sensitivity enables less post processing to be used, to save power for applications such as mobile devices. Applications include current sensors, built in current sensors, and IDDQ testing, even for next generation CMOS processes. Other variations can be envisaged within the scope of the claims.

CLAIMS:

1. A semiconductor device with a conductive element and a current sensor, wherein the current sensor is a magnetic current sensing device for sensing direct, varying or alternating current flowing through the conductive element, the current sensing device being integrated in the semiconductor device and being galvanically isolated from the conductive element.

2. A semiconductor device according to claim 1, suitable for measuring current with a μA resolution.

3. A semiconductor device according to any of the previous claims, wherein the current sensing device comprises at least one TMR device.

4. A semiconductor device according to claim 3, wherein the current sensing device has a free magnetic layer which has an easy axis oriented to be substantially perpendicular to a magnetic field caused by current under measurement.

5. A semiconductor device according to claim 4, the current sensing device having an easy axis, wherein the easy axis of the free layer is caused by shape elongation.

6. A semiconductor device according to any of claims 3 to 5, wherein the current sensing device is subjected to an additional magnetic field that can either be direct, varying or alternating.

7. A semiconductor device according to any of the previous claims, the current sensing device having a pinned magnetic layer with a magnetisation direction and a free magnetic layer having an easy axis, wherein the magnetisation direction of the pinned magnetic layer is oriented at an angle, with the easy axis of the free magnetic layer, preferably between 45° and 135°, more preferred substantially perpendicular to the easy axis of the free magnetic layer.

8. A semiconductor device according to any of the previous claims, wherein the sensor device is compatible with CMOS or MOS processing.

9. A semiconductor device according to any of the previous claims, wherein the semiconductor device is an integrated circuit.

10. A semiconductor device according to claim 9, wherein the current sensor or sensors are arranged to sense quiescent currents (IDDQ) or transient currents (IDDT).

11. Use of an integrated magnetic current sensing device which is galvanically not in contact with a conductive element, for sensing at least a direct, a varying or an alternating current flowing through the conductive element, wherein the sensing device is used for on-chip measurement of current.

12. Use of an integrated magnetic current sensing device according to claim 11, for sensing quiescent currents (IDDQ) or transient currents (IDDT).

13. A method for sensing current in a conductor in a semiconductor device, wherein the method comprises sensing a direct, a varying or an alternating current flowing in the conductor by performing contactless magnetic current sensing with a sensor integrated on the semiconductor device.

14. A method according to claim 13, wherein the method comprises sensing a magnetic field caused by the current.

15. A method according to any of claims 13 or 14, wherein the method comprises measuring current in at least one processing module.

16. A method according to claim 15, wherein the method comprises controlling the clock speed of at least one processing module to obtain a matching with a pre-defined current consumption level.

17. A method according to any of claims 13 to 15, wherein the method comprises the measurement of current consumption and the generation of a warning signal if a set current consumption threshold is superseded.

18. A method according to any of claims 13 to 15, wherein a software based routine performs job scheduling over several processing units based on the measured currents that invoke either an interrupt or a register bit to be set.

19. A software product which when executed on a processing device performs job scheduling over several processing units based on measured currents that invoke either an interrupt or a register bit to be set.

ABSTRACT:

A sensor for contactlessly detecting currents, has a sensor element having a magnetic tunnel junction, and detection circuitry, the sensor element having a resistance which varies with the magnetic field, and the detection circuitry is arranged to detect a tunnel current flowing through the tunnel junction. Anisotropy, such as caused by elongation, is oriented at an angle, preferably orthogonal to the magnetic field. Advantages include greater sensitivity. Also it can provide easy integration with next generation CMOS processes, including MRAM technology, be more compact, and use less power. The greater sensitivity enables less post processing to be used, to save power for applications such as mobile devices. Applications include current sensors, built-in current sensors, and IDDQ and IDDT testing, even for next generation CMOS processes.

Fig. 8A, 8B

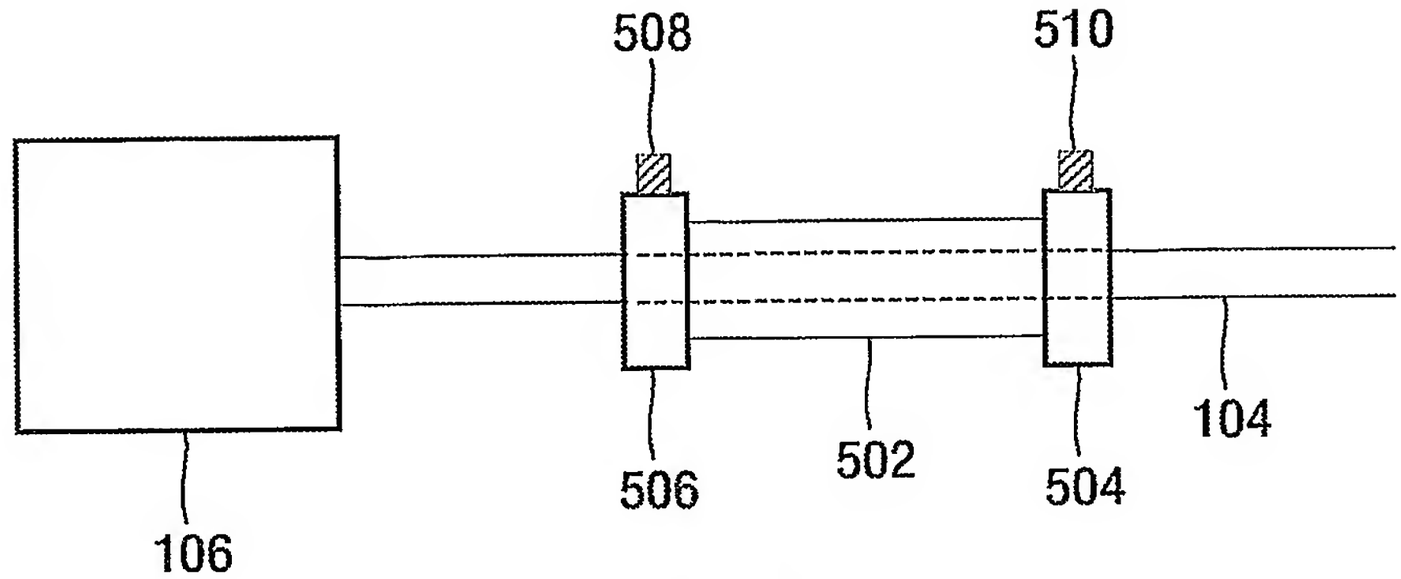


FIG.1
Priorart

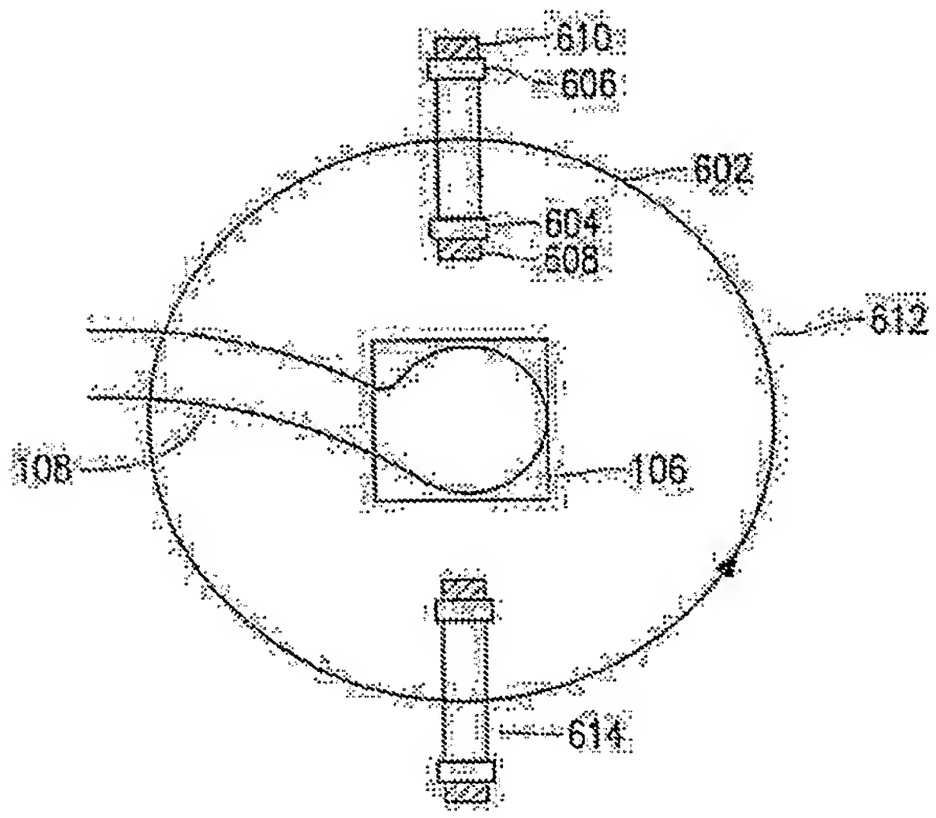


FIG.2
Priorart

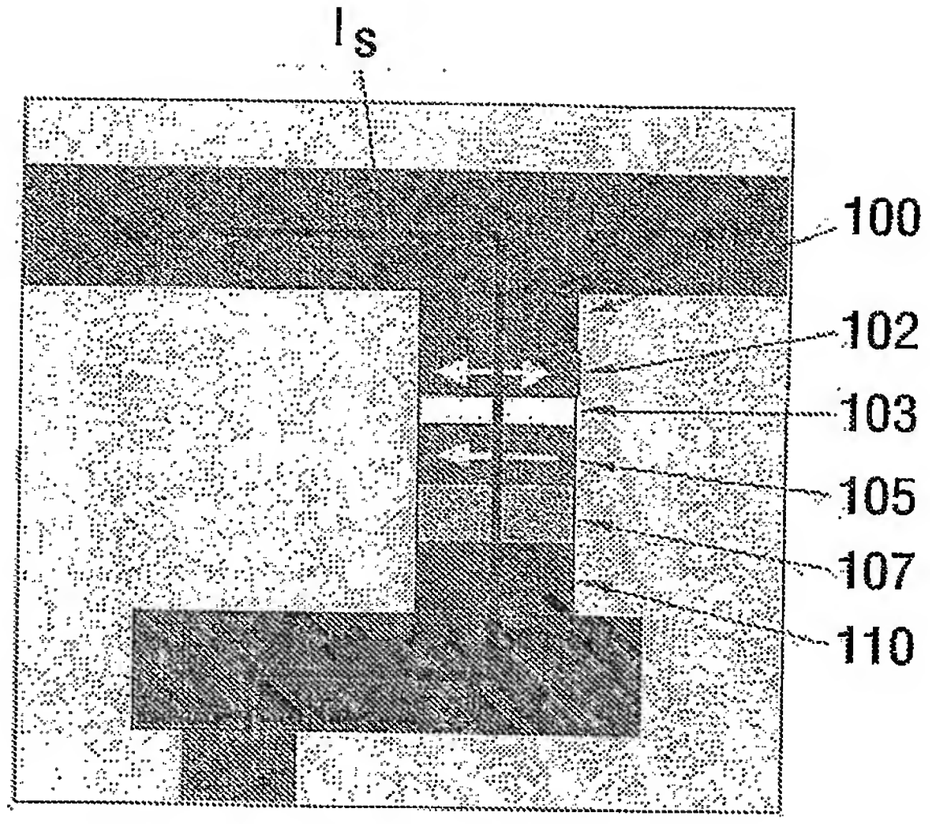
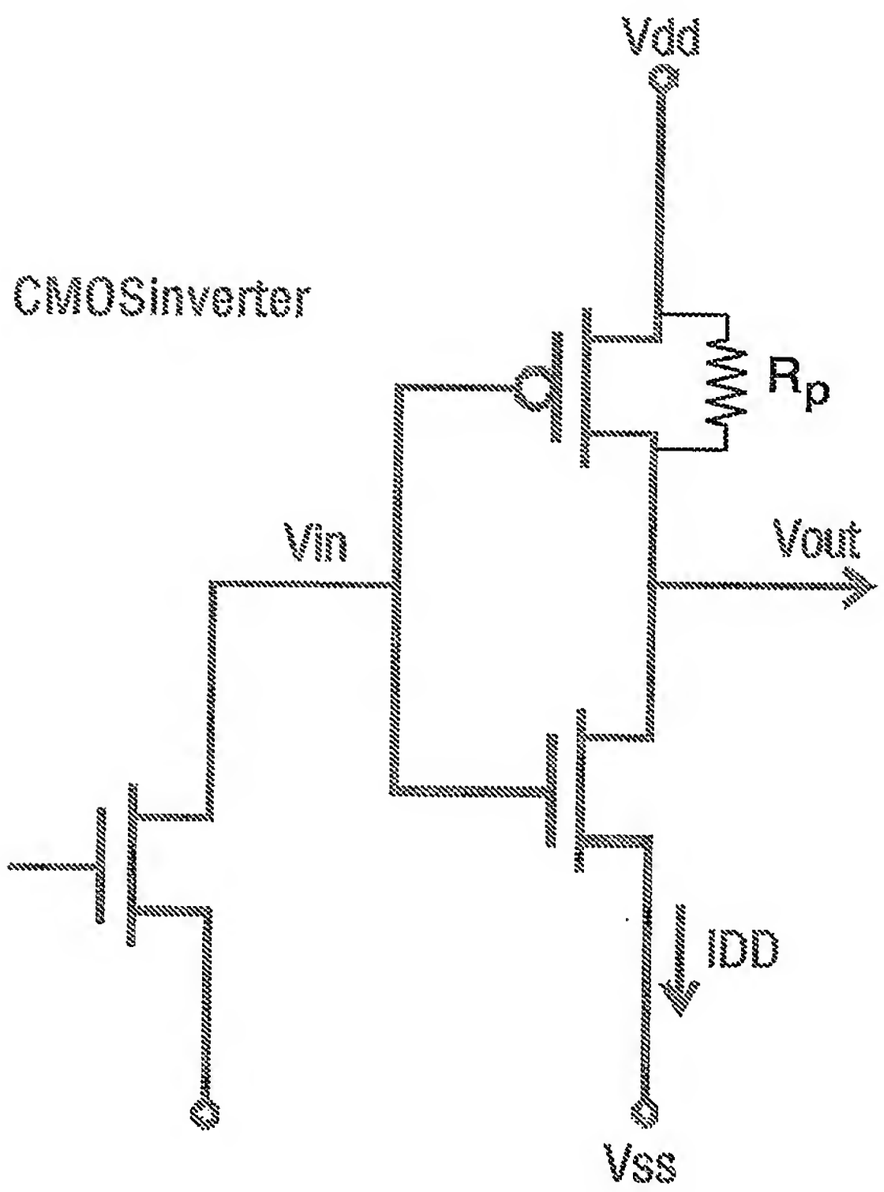
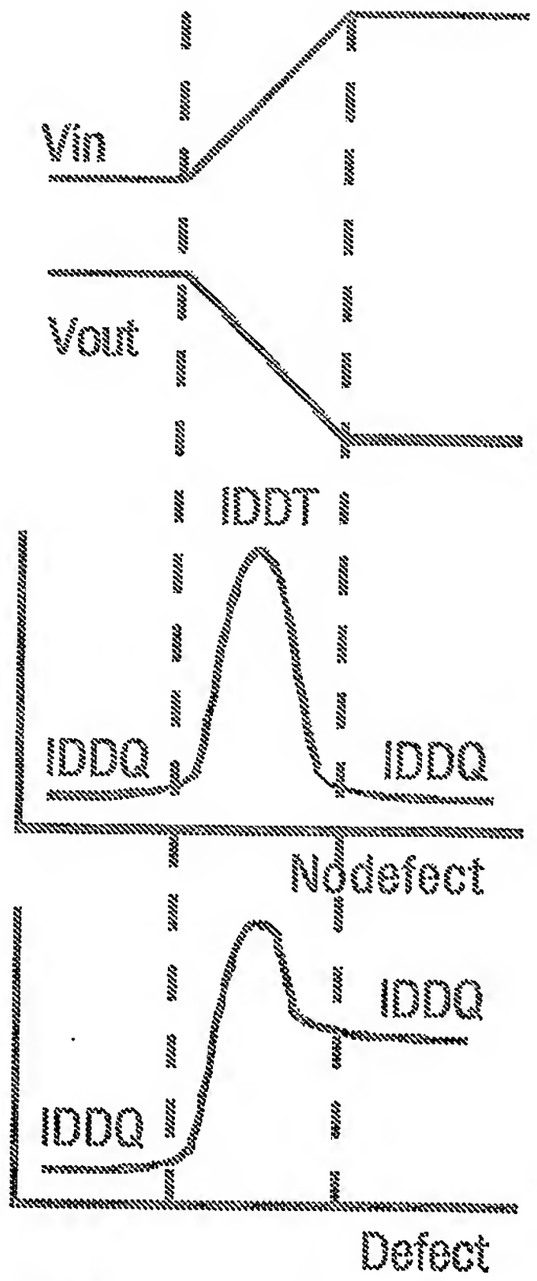


FIG.3





F I G . 4 A F I G . 4 B

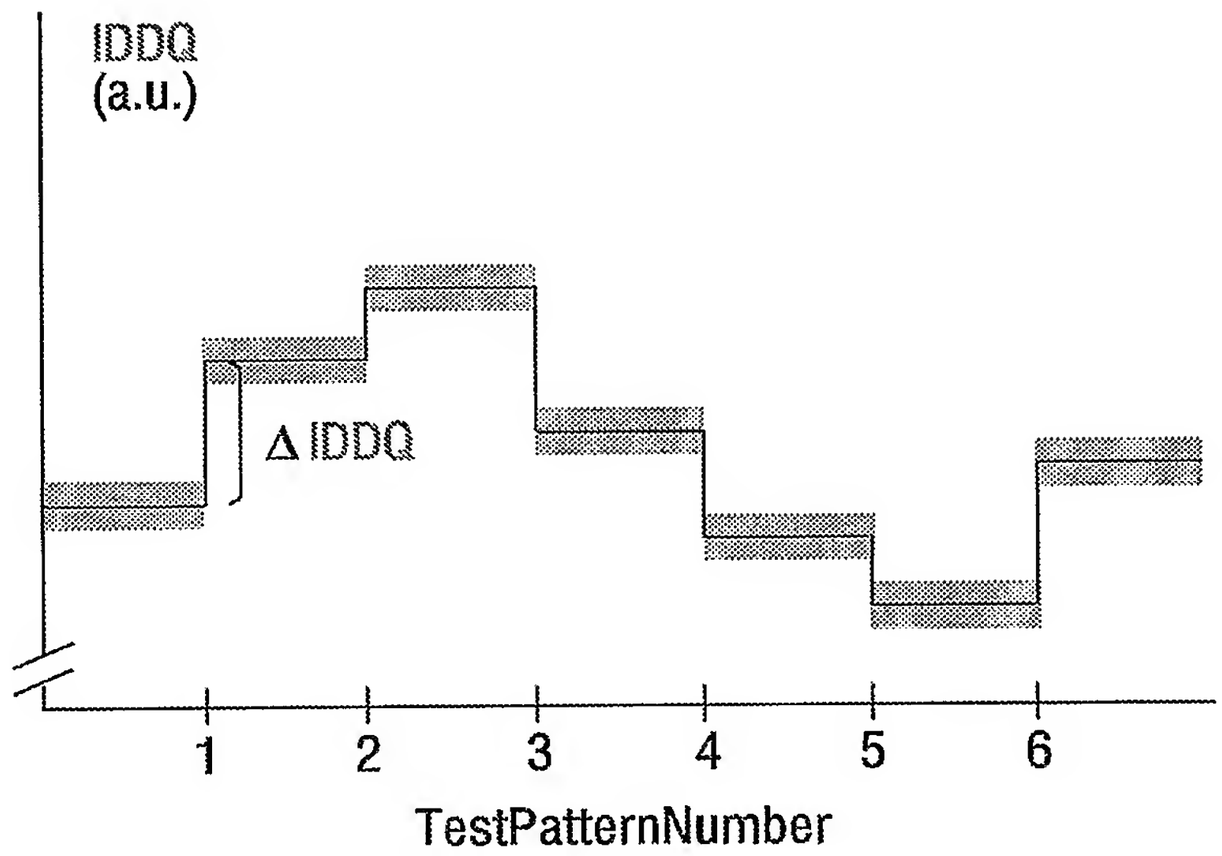

IDDQ
(a.u.)
ΔIDDQ
1
2
3
4
5
6
TestPatternNumber

FIG.5

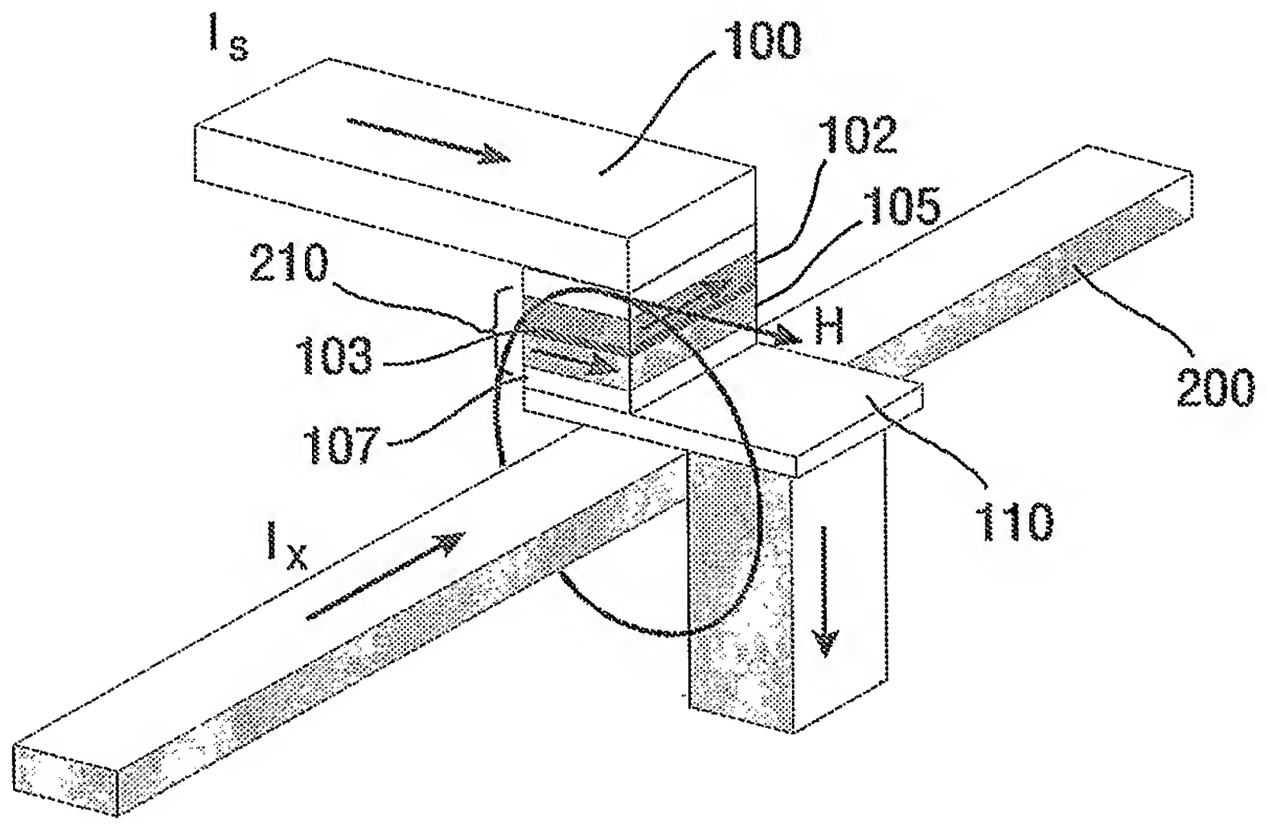

I_S
100
102
105
210
H
103
200
107
110
I_X

FIG.6

FIG. 7A

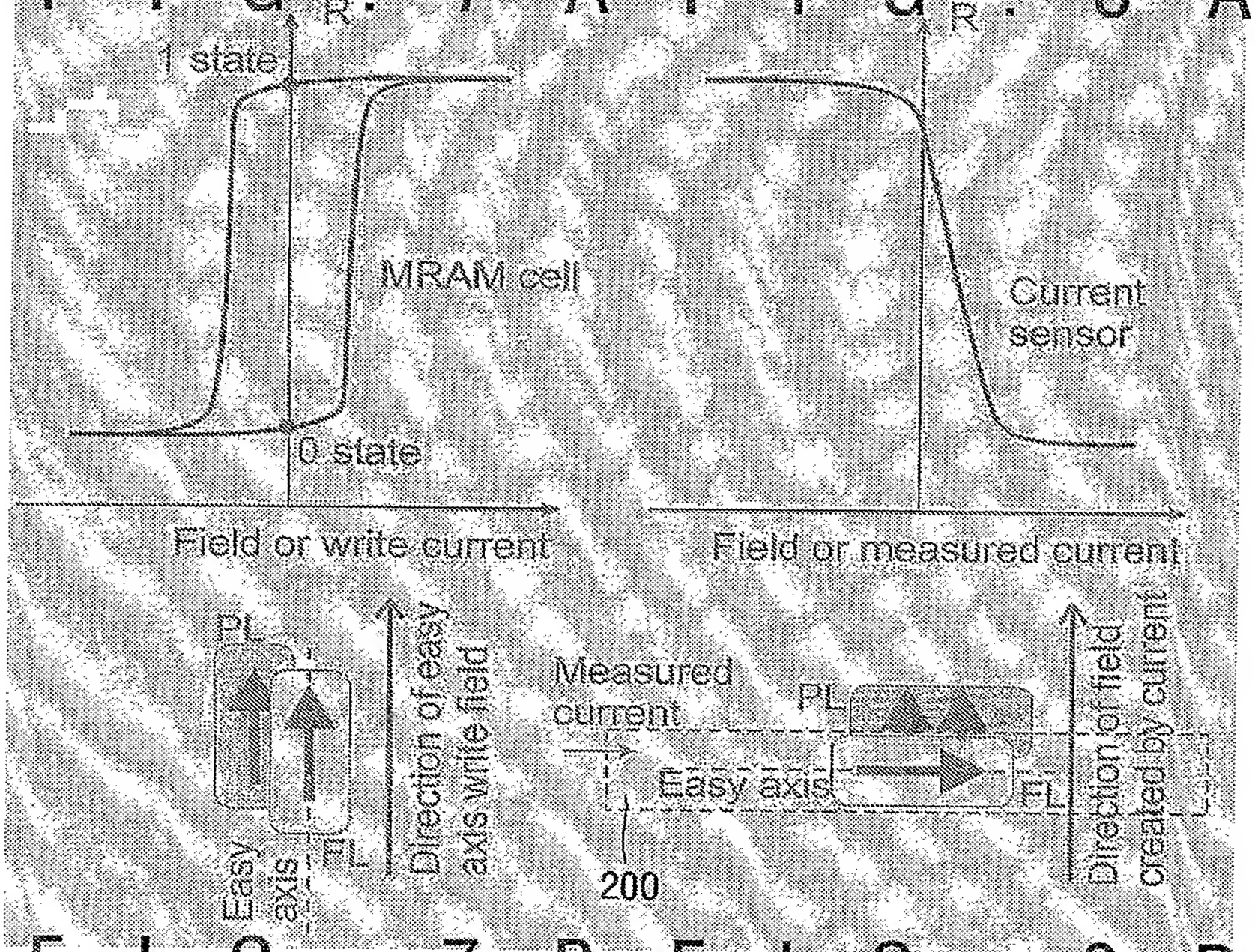


FIG. 7B

FIG. 8A

FIG. 8B

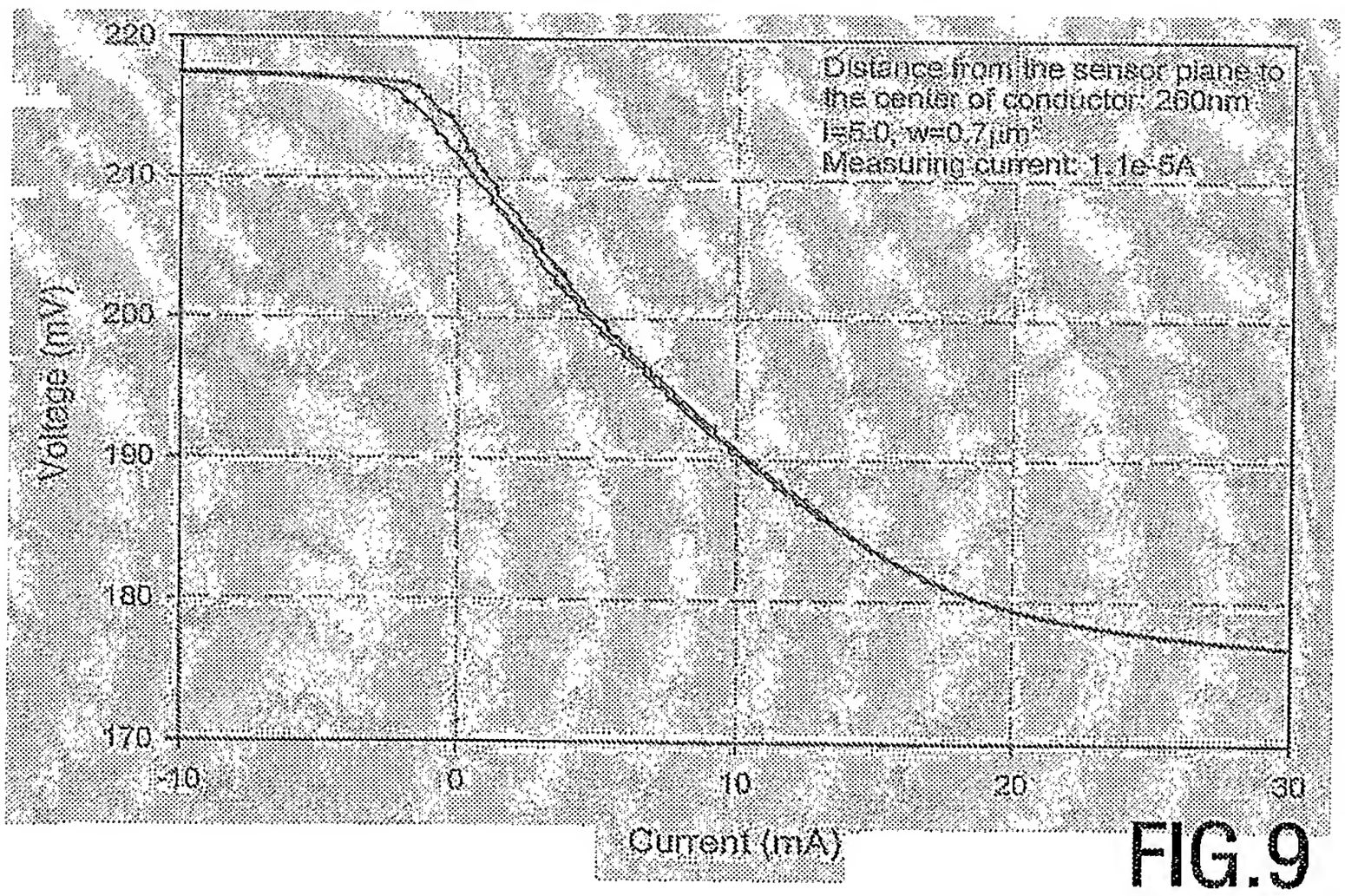


FIG.9

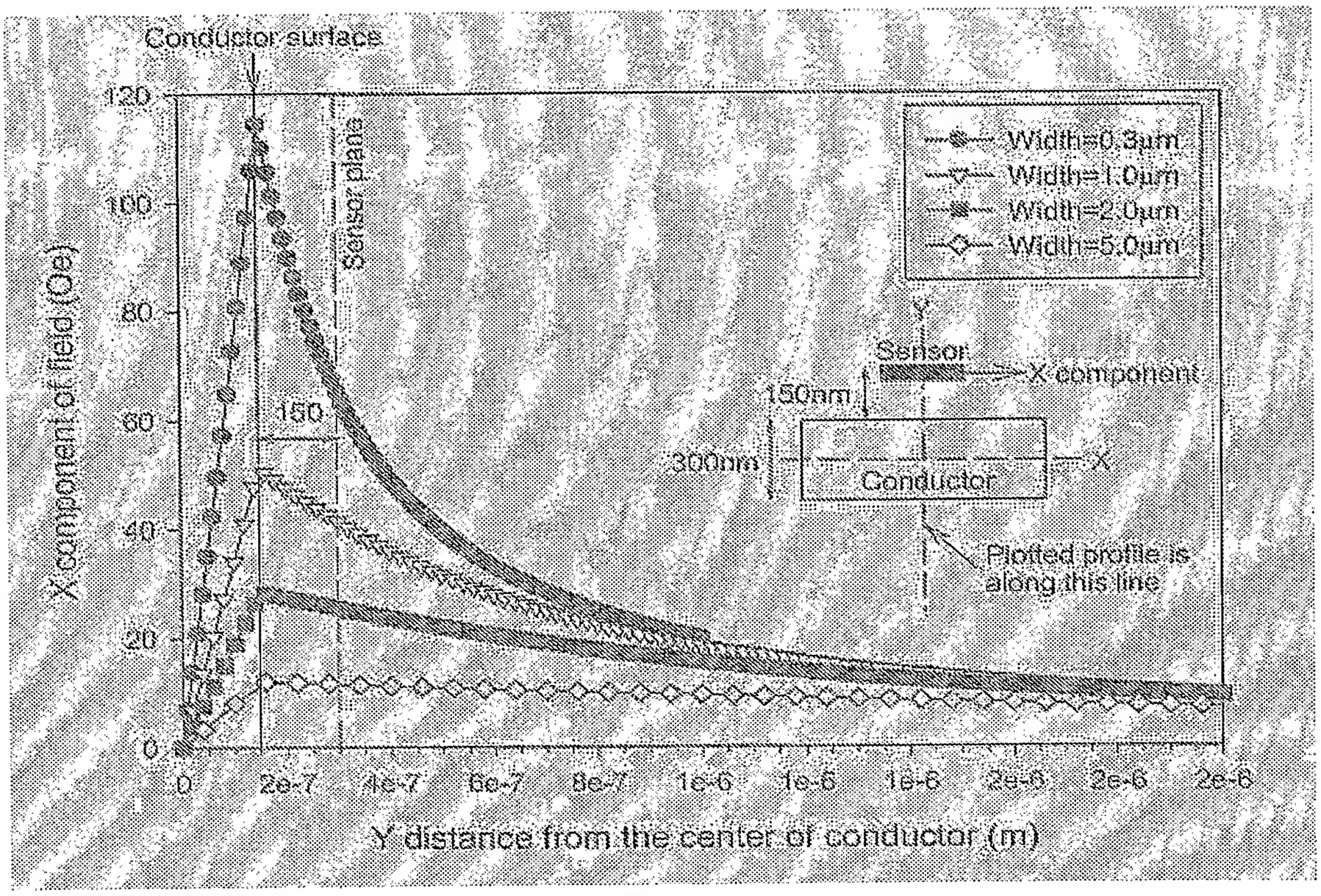


FIG.10

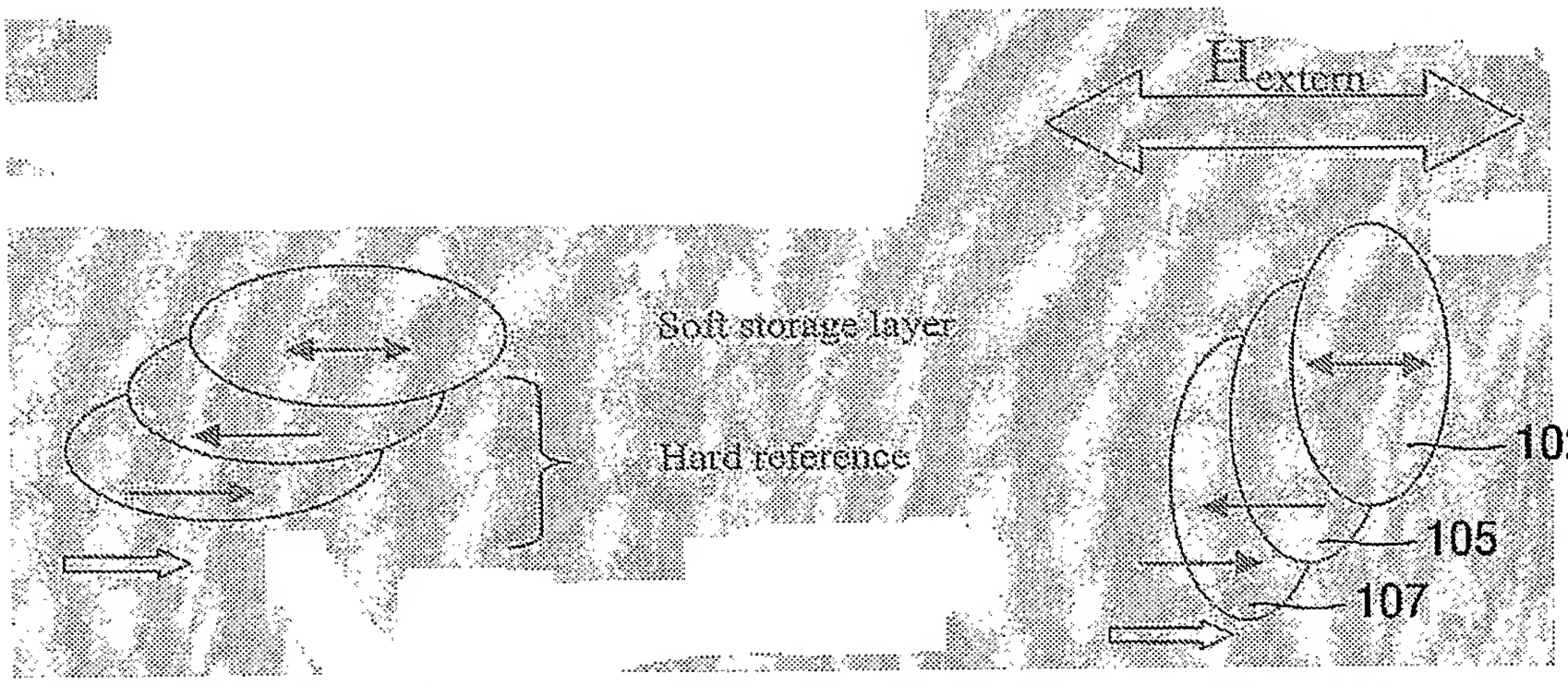


FIG.11

FIG.12

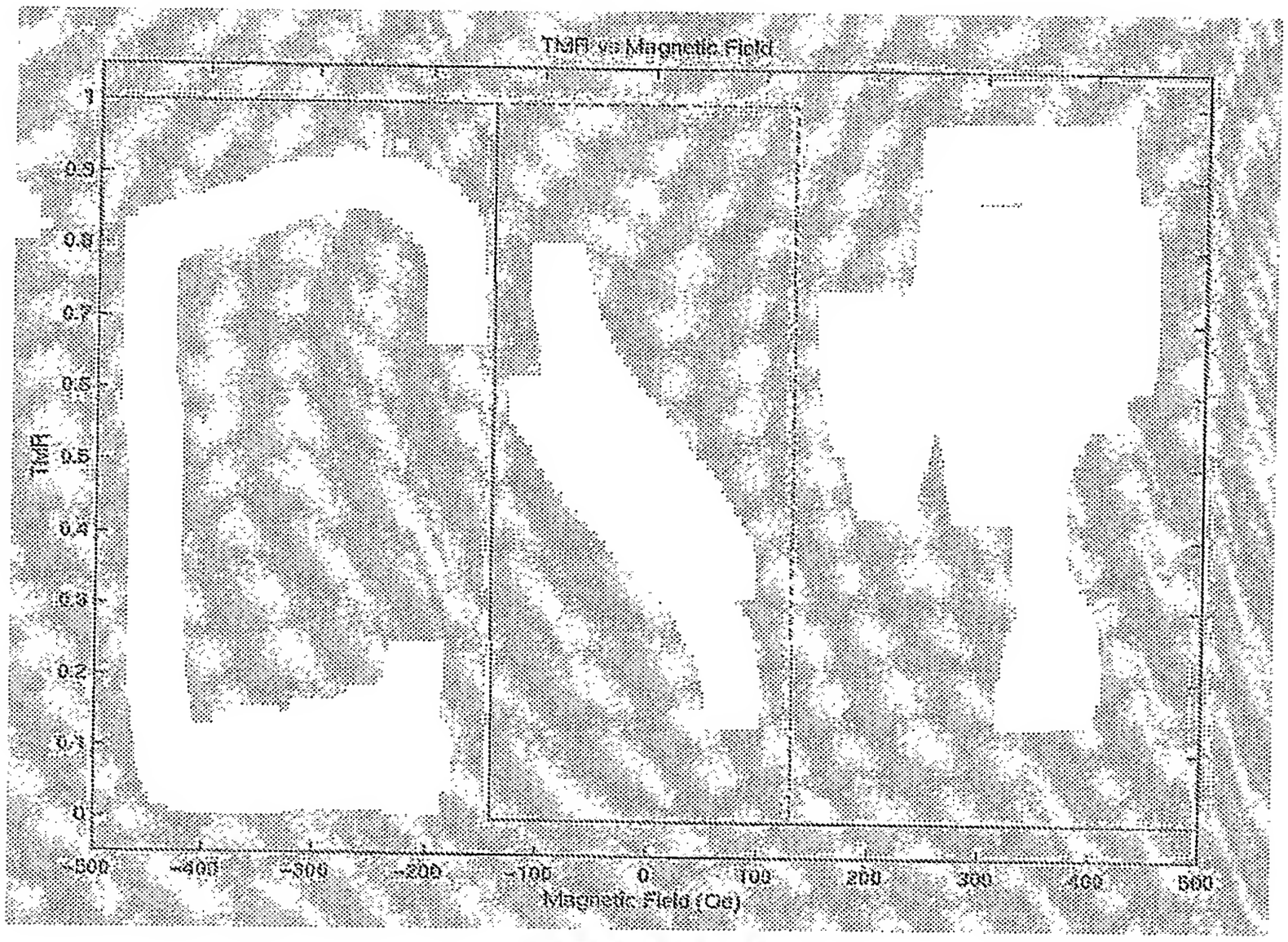

TMR vs Magnetic Field
TMR
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-500
-400
-300
-200
-100
0
100
200
300
400
500
Magnetic Field (Oe)

FIG.13

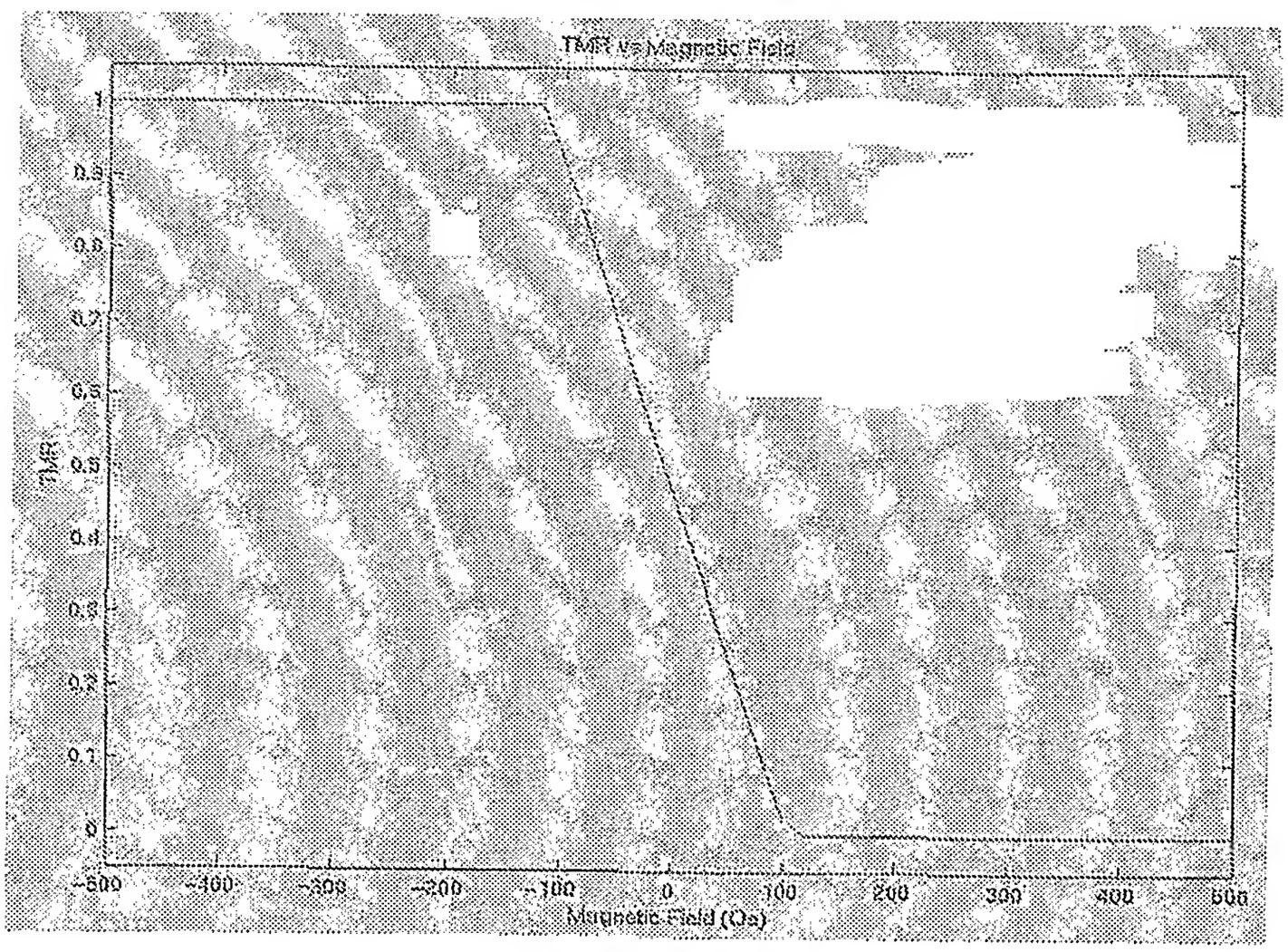

TMR vs Magnetic Field
TMR
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-500
-400
-300
-200
-100
0
100
200
300
400
500
Magnetic Field (Oe)

FIG.14

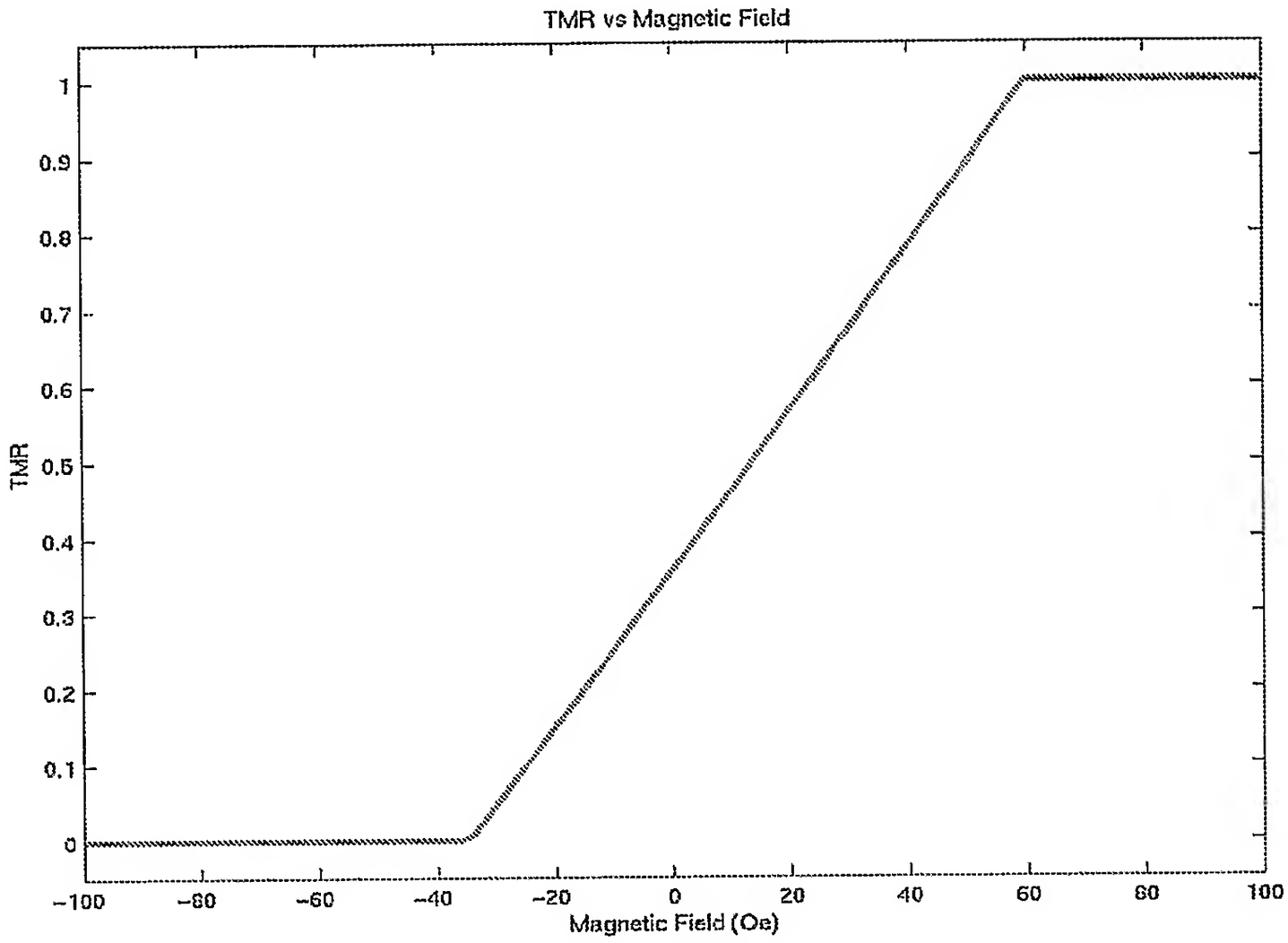

TMR vs Magnetic Field
TMR
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
−100
−80
−60
−40
−20
0
20
40
60
80
100
Magnetic Field (Oe)

FIG.15

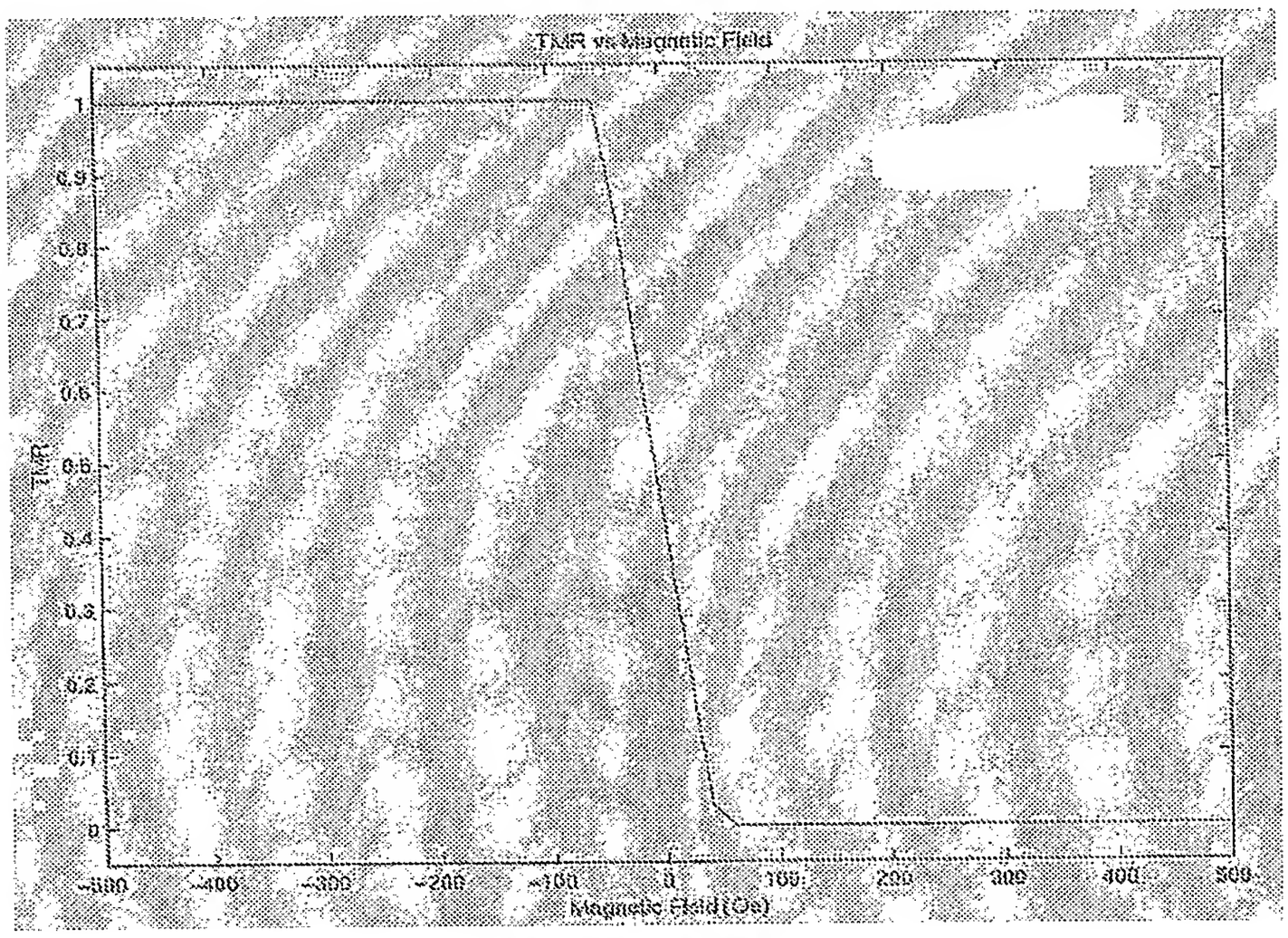

TMR vs Magnetic Field
TMR
Magnetic Field (Oe)

FIG.16

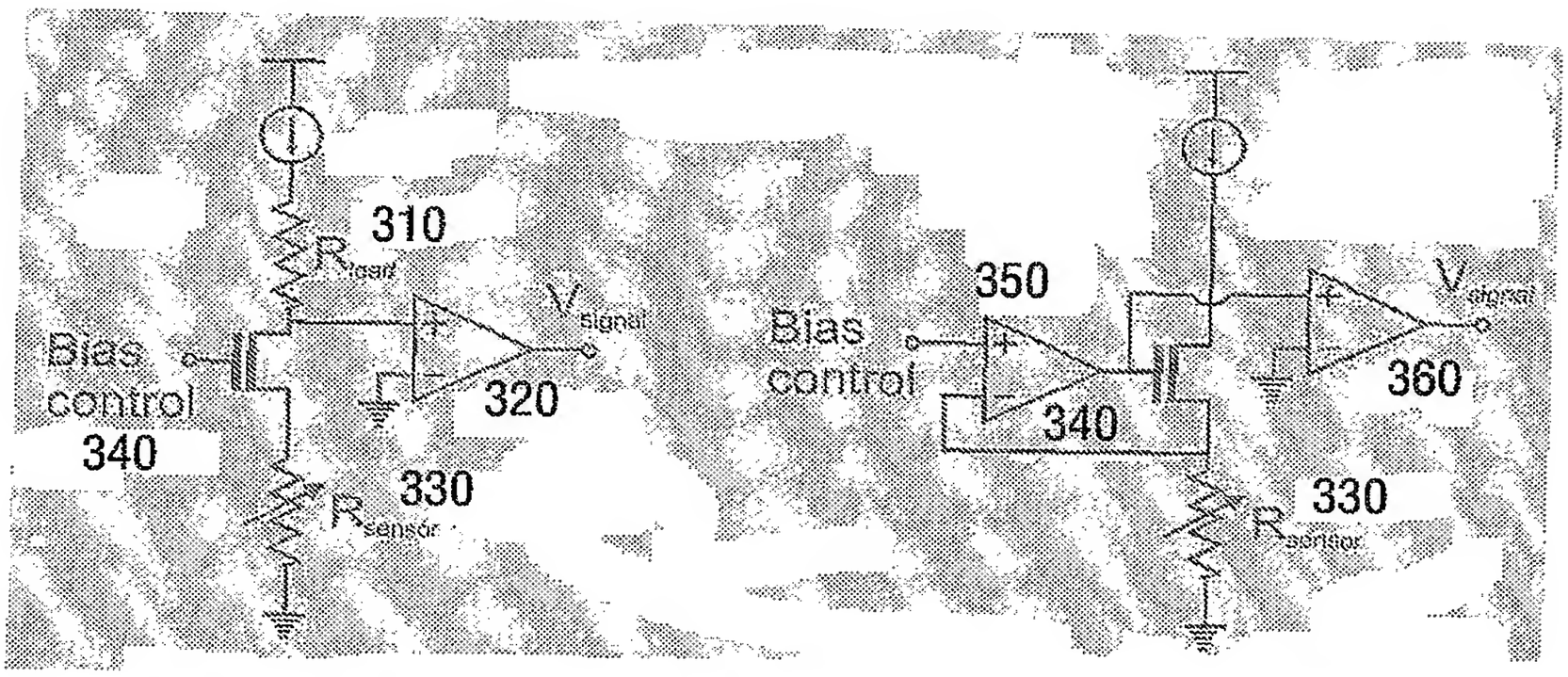


FIG. 17

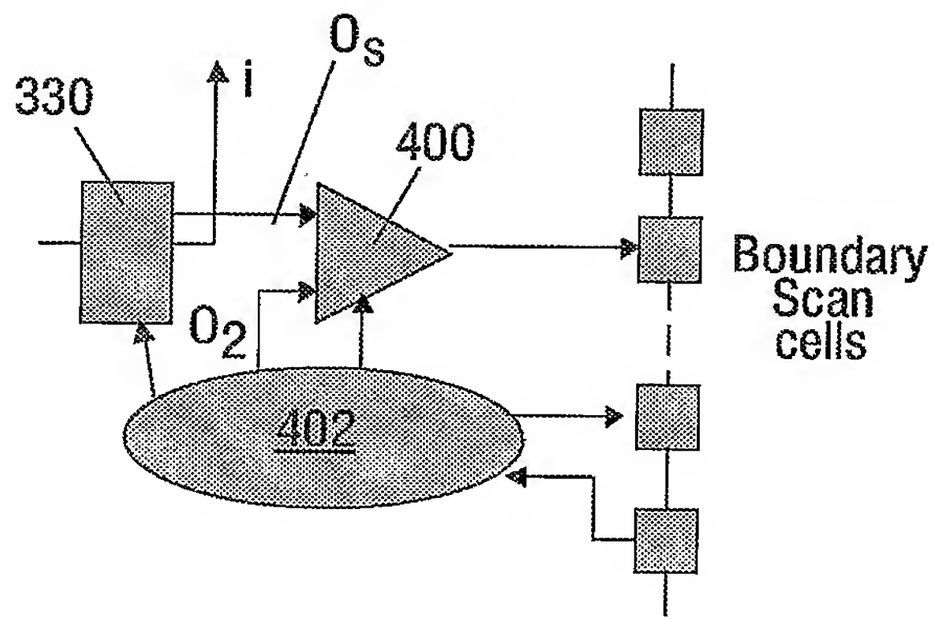


FIG. 18

FIG.19

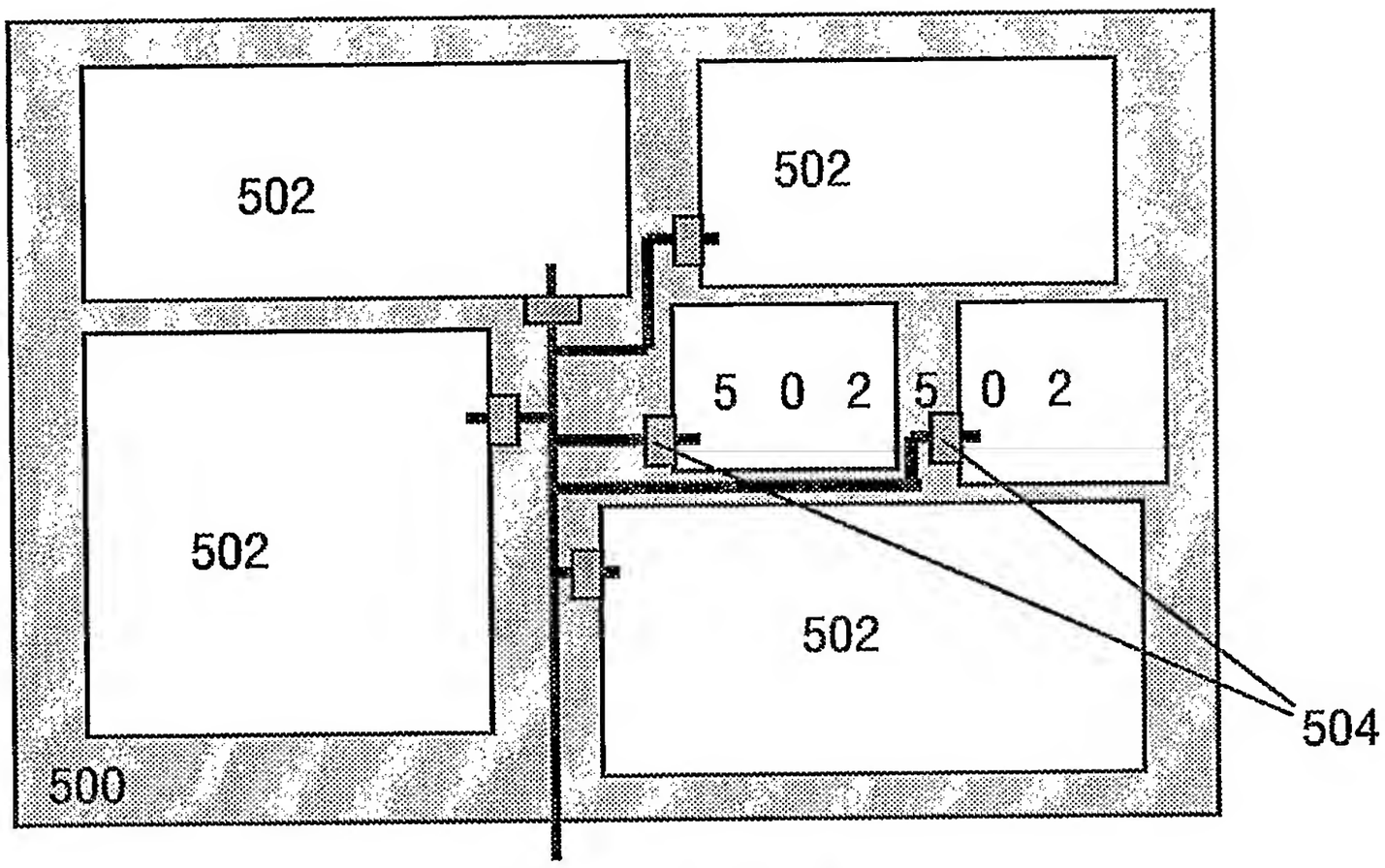


FIG.20

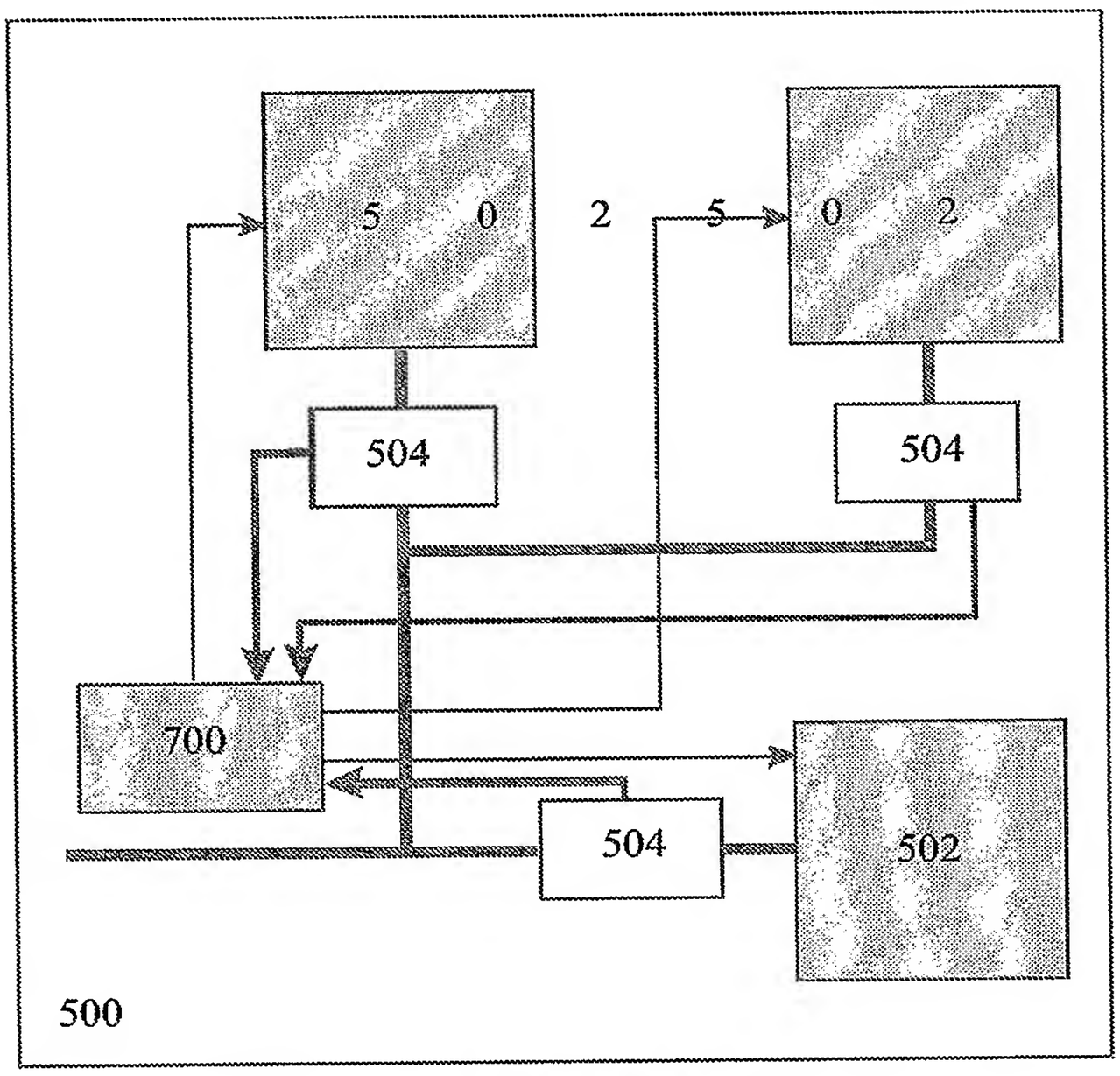


FIG.21